ABSTRACT

A system of interconnecting regions on an integrated semiconductor device or discrete components. As first connectivity layer has first and second runners to interconnect a plurality of first and second regions. A second connectivity layer has third runners to interconnect the first runners and fourth runners to interconnect the second runners. A third connectivity layer has first pads connected to the third runners and second pads connected to the fourth runners. Solder bumps are used on the first and second pads to connect the pads to other circuits.